

# SI2310

## 20V N-Channel Enhancement Mode MOSFET

**V<sub>DS</sub>= 20V**

**R<sub>DS(ON)</sub>, V<sub>GS</sub>@4.5V, I<sub>DS</sub>@5.0A < 28mΩ**

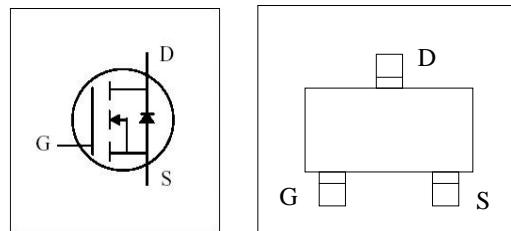
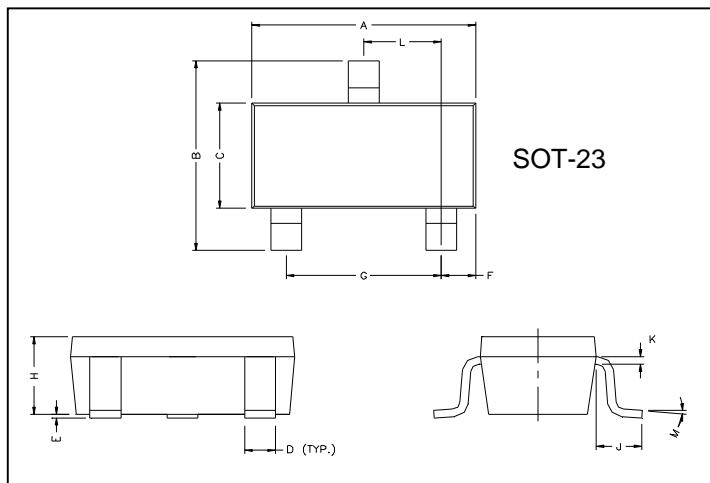
**R<sub>DS(ON)</sub> V<sub>GS</sub>@2.5V, I<sub>DS</sub>@4.5A < 35mΩ**

### Features

Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

### Package Dimensions



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.80	3.00	G	1.80	2.00
B	2.30	2.50	H	0.90	1.1
C	1.20	1.40	K	0.10	0.20
D	0.30	0.50	J	0.35	0.70
E	0	0.10	L	0.92	0.98
F	0.45	0.55	M	0°	10°

### Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 10$	V
Drain Current-Continuous	$I_D$	5.0	A
Drain Current-Pulsed (Note 1)	$I_{DM}$	13.5	A
Maximum Power Dissipation	$P_D$	1.25	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	°C/W

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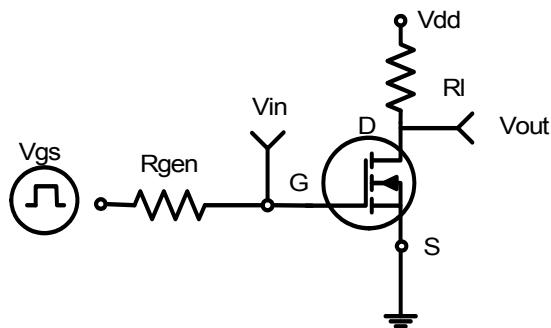
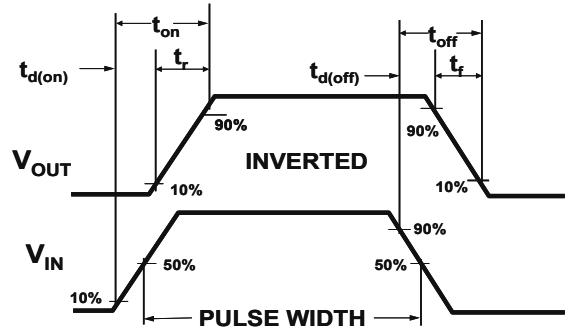
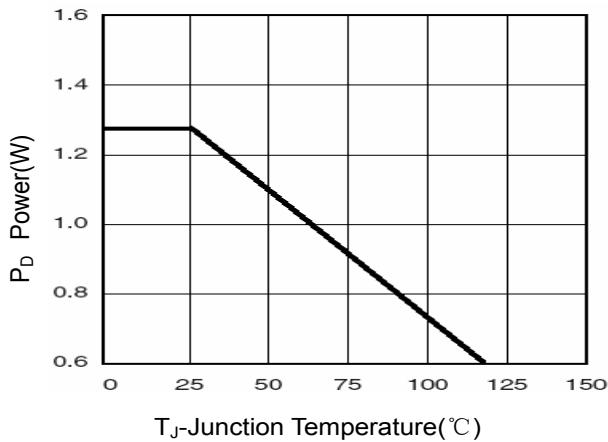


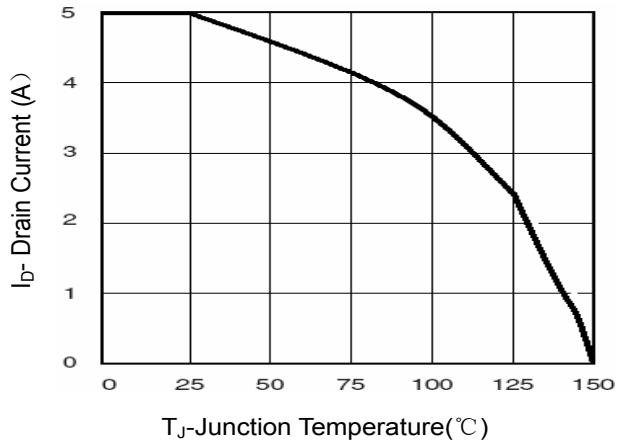
## Electrical Characteristics ( $T_A=25^\circ C$ unless otherwise noted)

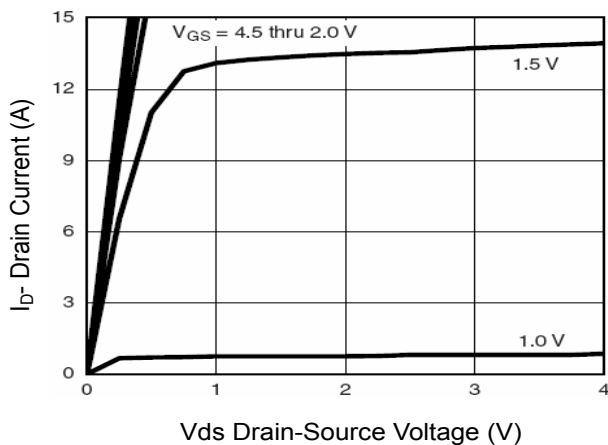
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	20	22	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=20V, V_{GS}=0V$	-	-	1	$\mu A$
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 10V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4	0.65	0.8	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=2.5V, I_D=4.5A$	-	27	35	$m\Omega$
		$V_{GS}=4.5V, I_D=5A$	-	20	28	$m\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=15V, I_D=5A$	-	25	-	S
<b>Dynamic Characteristics (Note 4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=10V, V_{GS}=0V, F=1.0MHz$	-	780	-	PF
Output Capacitance	$C_{oss}$		-	140	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	80	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=1A$ $V_{GS}=4.5V, R_{GEN}=6\Omega$	-	9	-	nS
Turn-on Rise Time	$t_r$		-	30	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	nS
Turn-Off Fall Time	$t_f$		-	10	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=10V, I_D=5A, V_{GS}=4.5V$	-	11.4	-	nC
Gate-Source Charge	$Q_{gs}$		-	2.3	-	nC
Gate-Drain Charge	$Q_{gd}$		-	2.9	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_s=2A$	-	-	1.2	V
Diode Forward Current (Note 2)	$I_s$		-	-	5	A

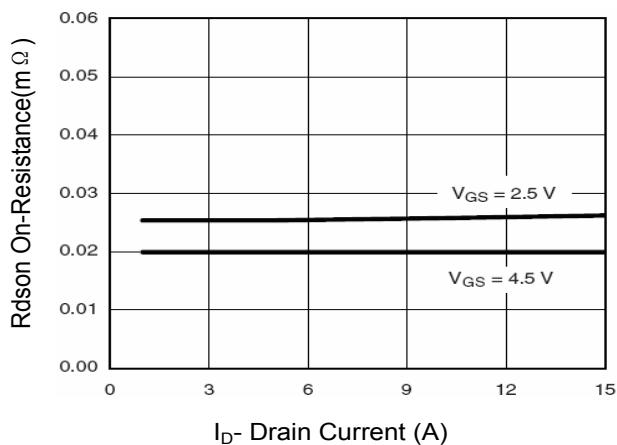
### Notes:

- 1.Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

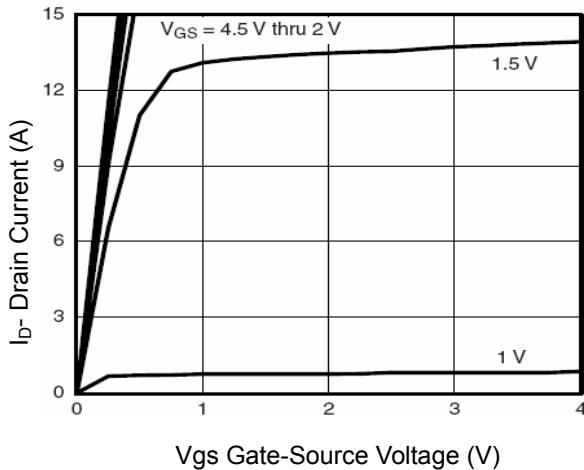
**Typical Electrical and Thermal Characteristics**

**Figure 1:Switching Test Circuit**

**Figure 2:Switching Waveforms**

T<sub>J</sub>-Junction Temperature(°C)

**Figure 3 Power Dissipation**

T<sub>J</sub>-Junction Temperature(°C)

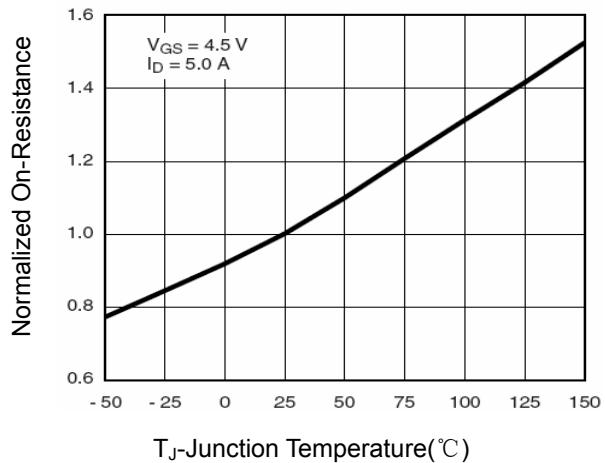
**Figure 4 Drain Current**

V<sub>ds</sub> Drain-Source Voltage (V)

**Figure 5 Output Characteristics**

I<sub>D</sub>- Drain Current (A)

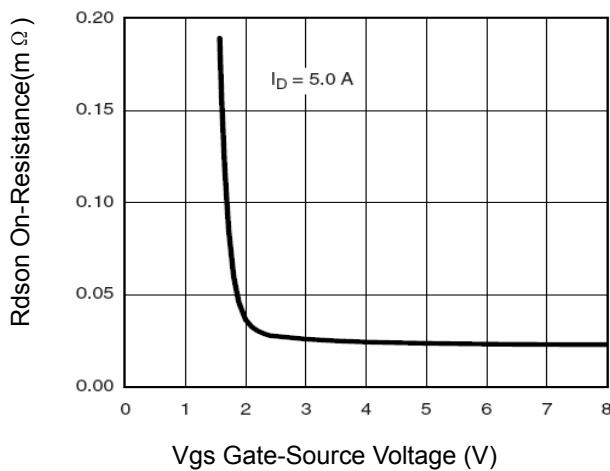
**Figure 6 Drain-Source On-Resistance**



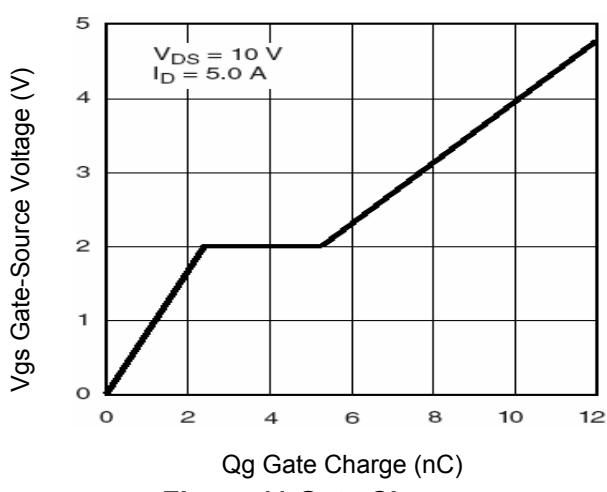
**Figure 7 Transfer Characteristics**



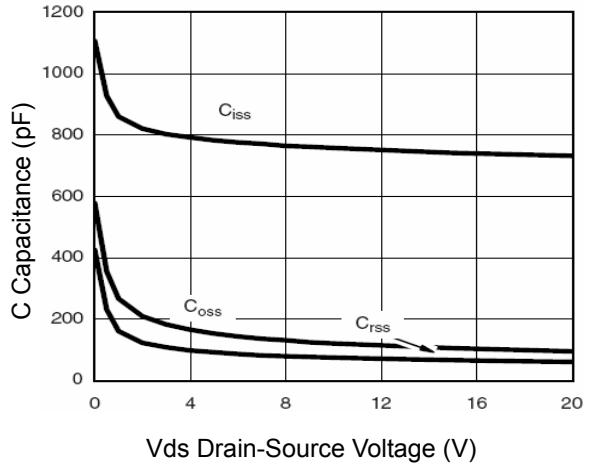
**Figure 8 Drain-Source On-Resistance**



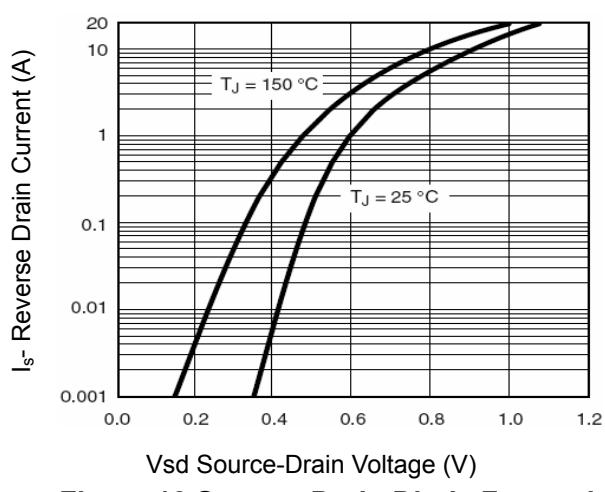
**Figure 9  $R_{DS(on)}$  vs  $V_{GS}$**



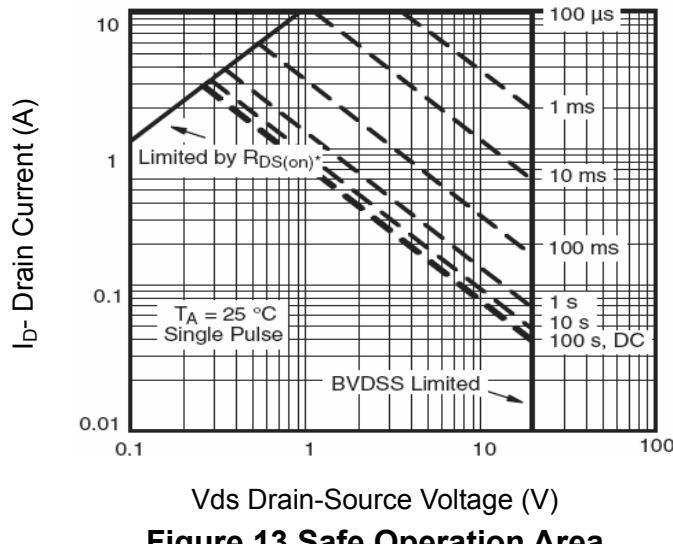
**Figure 11 Gate Charge**



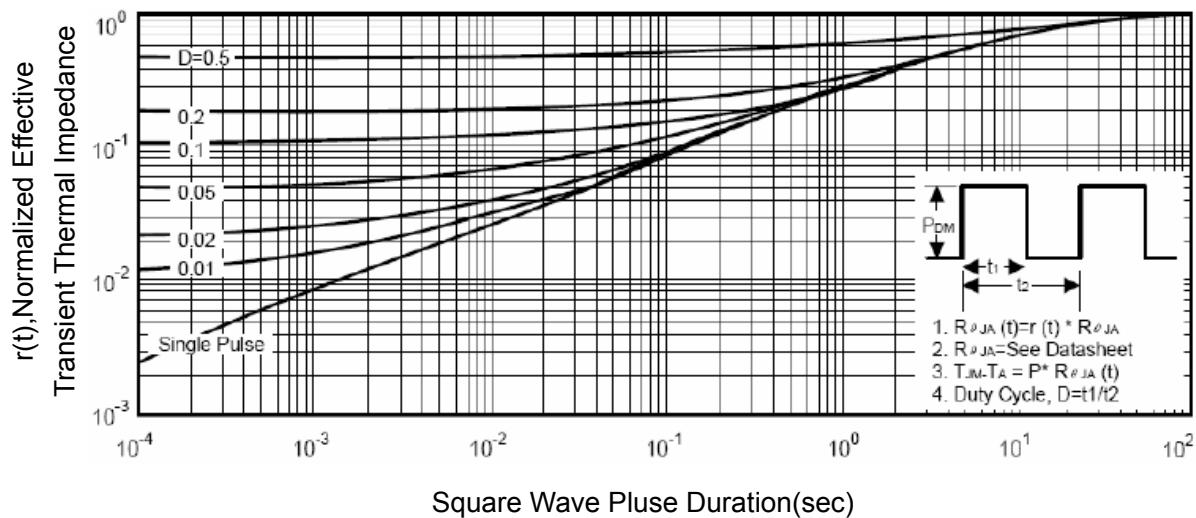
**Figure 10 Capacitance vs  $V_{DS}$**



**Figure 12 Source- Drain Diode Forward**



## **Figure 13 Safe Operation Area**



**Figure 14 Normalized Maximum Transient Thermal Impedance**